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Digital Down Converter for 5G systems

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Research Article

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Abstract: The creation of 5G system designs is a current topic in VLSI and communication research. The designed architectures must be both operationally efficient and compliant with the 3GPP's proposed standards. A digital down converter is one of the main components of a 5G receiver. The intermediate frequency must be converted to baseband frequency by this unit. A few recent developments in this area are summarized in this publication.

Keywords: Digital Down Converter; 5G; Communication; Survey

I.INTRODUCTION

The fifth-generation technological standard for broadband cellular networks is known as 5G. It is intended to enhance the wireless devices' flexibility, speed, and latency.Higher, less crowded radio frequencies are used by 5G. As a result, it can transmit more data much more quickly.

An RF, an IF, and a baseband part make up a communication system. Demodulation, decoder modules, and IF conversion to baseband frequency are all included in the baseband portion.

By reducing the input signal to a lower sample rate, the Digital Down Converter (DDC) module, which transforms IF to baseband, enables lower-speed processors to handle incoming rapid signals. The DDC is used in radio receivers and carries out the essential task in communication systems. Field-programmable gate arrays or application-specific integrated circuits are used to implement it.

This work's primary objective is to decrease the DDC's space and power consumption in order to improve the baseband section's overall efficiency by altering the filter and oscillator topologies.

In this work, we alter the FIR filter's design to use fewer multipliers and adders. Lastly, the power, area, and speed numbers for the current and suggested architecture are computed, and simulation results are shown.

LITERATURE SURVEY

The proposed architecture of transceiver uses digital design of the receiver and transmitter intermediate stage. The implementation of the transceiver by digital intermediate frequency stages (DUC/DDC) brings new quality to the professional transceivers which enables to minimize implementation losses compared to analog systems. The advantage of using DUC and DDC are unmatched quality of modulation signal and good manufacture repeatability, a receiver can be implemented without linear distortion of the processed signals respectively. The modulated signal quality is better than at the transceivers with classical analog angular modulators.

The drawback of the proposed digital design could be higher power consumption as compared to the analog system because of the passive filters used and also the use of an A/D and D/A converter limits the performance.

This paper presents a quadratic Digital Down-Conversion (DDC) structure which moves Intermediate Frequency (IF) signal to baseband by two steps. Firstly, IF signal is passed to baseband nearby using a structure based on polyphase filter. This structure places mixers after polyphase filters. Then, the signal is passed to baseband through conventional orthogonal frequency mixing. This architecture can reduce filter resources and effectively reduce the sample rate and process cost by improving the operation efficiency. Also, this paper analyses the way of implementing the complex coefficient filters resulting from the prepositive filter structure.

However, the digital filter with complex coefficients is introduced with the quadratic DDC structure, which makes the quadratic structure difficult to implement on FPGA to some extent.

The radar system consists of a transmitter and a

receiver, where the transmitter reflects from the object and returns to receiver with some information about an object. All the received signals from the receiver should be pre-processed prior sending it to the signal Processing stages. Here DDC is used for pre-processing the signal. The disadvantages of DDC using single stage FIR filter are made to overcome using Multistage FIR filter approach, which is more efficient. The main aim of the proposed methodology would be to implement the DDC on FPGA (Virtex-5) which as advantages in areas of hardware complexity, speed and power dissipation.

The downside of this proposed system will be the area penalty for field programmability and expensive production volume FPGA.

In this polyphase digital down-conversion method, the high-speed sampling input signal and the oscillation signal are parallelized, then to decrease the speed of the incoming signal, the input signal is decomposed to M sub-channel by polyphase decomposition. The digital down-conversion operation is executed for every channel of input signal data and by the poly phase filtering, down-conversion of the high-speed sampling signal can be carried out at low sampling speed signal. Later the simulations are performed to check the efficacy of this method.

The disadvantage of using polyphase digital down- conversion method is, it requires a large amount of hardware resource.

PROPOSED METHODOLOGY

The architectural block diagram of DDC is shown in Fig. 1. To make the design efficient individual architectures such as NCO and FIR circuits must be modified.

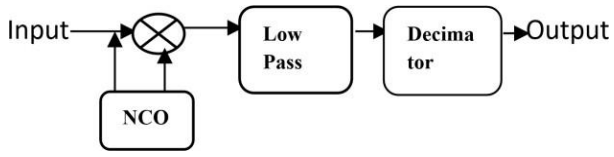


Fig 1. Architectural block diagram of DDC

CONCLUSION

This study investigates innovative oscillator and filter structures. By altering the filter design, fewer filter coefficients are produced, which lowers power and area usage. We will be able to overcome the shortcomings mentioned in the literature review by using the suggested system, which also improves the system's speed and efficiency.

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