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Distinct ρ-based model of silicon N-channel double gate MOSFET

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Abstract

Metal-oxide-semiconductor (MOS) technology is used in the fields of very large scale integrated (VLSI) circuit technology to meet the ever-increasing need for digital processing technology. This technology allows for high-speed calculations with little propagation delay and low power consumption. However, in the current microelectronic regime, MOS technology is having trouble linearly scaling transistors with various channel modeling. Short-channel effects (SCEs) limit the MOSFET's linear scalability. With its variable input capacitance value ratio and appropriate forward transfer admittance, silicon N-channel double gate MOSFETs (DG MOSFETs) are used in the modern microelectronic regime to achieve the short channel effect of MOSFETs. In order to estimate the varying junction capacitances that can limit the use of intrusion detection systems (IDS) in VLSI applications, a unique ρ-based model is developed in this research paper to simulate SCEs using silicon N-channel double gate MOSFETs with varying front and back gate doping levels and surface regions. A simulated model for the total internal device capacitance using a different ρ-based model and an analytical model for the channel length are shown. Comparative findings demonstrate the efficacy of the suggested unique ρ-based model, which is appropriate for silicon nanowire transistors.

INTRODUCTION

1. According to Moore's Law, the silicon-based semiconductor sector is growing quickly in the contemporary period and is essential to the design of integrated circuits, wireless communication systems, mobile devices, and other gadgets. These semiconductor sectors are now exploring various materials and technologies to meet the needs of power, cost, area, and speed in high integration density applications due to scientific and technological advancements. Further, silicon on insulator (SOI) devices [2], which can be scaled more aggressively than bulk CMOS, are an alternative to complementary metal-oxide-semiconductor (CMOS) [1], which is confronted with basic physical limitations in terms of circuit, device, and material. Despite having the same substrate, material, and manufacturing method, SOI and its derivatives, partly depleted (PD) and completely depleted (FD), are very vulnerable to floating body effects due to scaling limits, which results in the threshold
2. voltage that is sensitive to the device terminal interface and SOI thickness. The best substitutes for SOI are advanced MOSFET structures, including multiple gate MOSFETs, which can scale bulk SOI architectures. In contrast to bulk MOSFETs, a double gate MOSFET (DG MOSFET) structure manufactured on an SOI wafer is used in [6]. The DG-MOSFET is a significant device among the developing MOSFETs [7], as shown by [8], [9]. The following are the issue statements that this suggested paper DG MOSFET design addresses based on the reviewed literature: i) Four-terminal driven DG-MOSFETs have an unfavorable subthreshold slope, which is a limitation brought on by the fixed second gate voltage [10]. ii) The restriction resulting from a reduction in oxide width with high doping levels in the device substrate; iii)

The minimum channel length imposed by short-channel effects is associated with four times the thickness width of the oxide layer. The subthreshold volume inversion is caused by an increase in junction capacitance and current tunneling, as well as a slope of subthreshold current and carrier mobility in the device drain [11] terminal; iii) Limitation resulting from the subthreshold's slope, which permits the device to reduce leakage current in the device through driving current [12], lowering the threshold voltage with the falling subthreshold slope in a channelled DG MOSFETs; and iv) Limitation arises as the top gate is conducted and causes the short-channel effect [13]–[15]. Because tri-gate MOSFETs' short-channel effects (SCEs) are more controllable than those of FinFETs, the double-gate design raises the device's gain, which lowers SCEs.

In this study, the design of DG MOSFET devices has been implemented in several scenarios [16]–[18] by adjusting the channel length and balancing linearity, power, and speed performance. The scaling is done using the scaling constant values and the supposition that the device is dimensionally smaller. A new distinct ρ-based DG-MOSFET architecture model is to be proposed and designed, and the characteristics of the four-terminal driven DG MOSFET are to be investigated in relation to the proposed distinct ρ-based DG-MOSFET architecture model. Additionally, the short-channel effects will be analyzed using a current continuity equation based on Poisson's equation. A overview of earlier techniques is presented in section 2. Section 3 presents the suggested DG MOSFET's modeling and technique. The suggested DG MOSFET's simulation results and comments are presented in section 4. The results and future scope of the suggested study are presented in Sections 5 and 6.

3. LITERATURE REVIEW

A FinFET transistor with multi-gate device, having higher performance, the challenges of FinFETs are: a) By decreasing the fin-width, SCEs are reduced via the fin shape, and subthreshold fluctuations are reduced by lowering the doping level in the channel. The gate on the sides and top electrostatic impact will be lessened for FinFETs that are too thick. Variability might also result from a lack of fins. The use of discrete-sized high dielectric grain layers in DG MOSFET channel doping presents a fin doping difficulty. [19]–[23]. DG MOSFETs function optimally when arranged in regular grid configurations. Through unique variants, grains are added as discrete sized high dielectric grain layers to boost gate drive strength, which FinFETs can not provide. Because of the inherent properties of FinFET technology, channel length variation and body biasing have a limited value. This may be mitigated by using discrete-sized high dielectric grain layers in DG MOSFETs. b) The charge sharing takes place at the corners of the front and rear gates due to the close closeness of the gates in FinFET, causing an early inversion of the gate-to-channel electric field. The use of distinct grains at the middle of gates, where the high dielectric grain layers are positioned at a constant (ρ) and equal position locations with a discrete size during DG MOSFET channels doping from its surface to channel location, and the difficulty of subthreshold characteristics of the FinFET degrades are all addressed. The gate of a double gate MOSFET is composed of aluminum, whereas the source and drain are composed of silicon. the application of high dielectric grain layers in the strained Si materials at equal and constant (ρ) position sites. Because it maintains a respectable degree of electron and hole mobility even at lower thicknesses, the material utilized for grains is scalable. Grain-based MOSFETs are capable of becoming high-performance semiconductor devices. The Gate Oxide material's thickness is raised to decrease leakage currents as they rise. A comparatively high dielectric grain layer material is used in lieu of silicon dioxide, which has a lower relative dielectric constant, to boost gate capacitance. In order to lower the leakage current across the structure, a thicker dielectric gate layer will be able to be employed.

Such a unique ρ-based model of silicon N-channel double gate MOSFET with high dielectric grain layers at constant (ρ) and equal position compact models must have subthreshold swing, modulation of channel length, and dependence on short channel effects on threshold voltage with temperature and structure dimensions. Lastly, they must to be precise and computationally effective.

4. PROPOSED DISTINCT ρ-BASED DEVICE MODEL AND METHODOLOGY

This section discusses the theoretical and practical models for the modeling of the proposed unique ρ-based device. MATLAB code has been presented to demonstrate the analytical model of proposed device design and the Distinct ρ-based device design model is adopted to implement Silicon N-channel dual-gate MOSFET. The models for short and long channel DG MOSFET are categorized into electrostatic surface charge distributions, total internal device capacitance and device drain-source characteristics models for analytical and simulation models [24], [25]. In this research work, planar DGMOSFET is considered with a distinct ρ-based device, which is an alternative technology for FinFET's. The performance of IDS and DIBL is better than that of GAA and Tri-gate MOSFETs. In this paper, a conventional, one top gate DG MOSFET and both gate DGMOSFET's are considered with gate all around (GAA), FinFETS, and tri-gate MOSFETs. For 10 nm scale, the performance of proposed DGMOSFET is showing an improved ΔVg a varying gate voltage for different front and back gate voltages. Study and implementation of proposed DG MOSFET through planar design can be made relevant with the usage of doping concentration structures, where resistance can be reduced, inturn increasing the IDS for improved swithching action. In this research paper, a layered DG MOSFET structure through ballistic quantum simulation is introduced. This layered structure with distinct slots structure solutions is presented through Poisson continuity equation in making ballistic electrons. Using MATLAB, the proposed layered DG MOSFET with device structure and doping levels are analyzed.

4.1. Distinct ρ-based device structure

The structure of the proposed distinct ρ-based DG MOSFET used in this research work is schematically presented in Figure 1, have the design parameters as shown in Table 1. In the defined structure, symmetrical p+ and p- poly gates without drain and source device terminals.

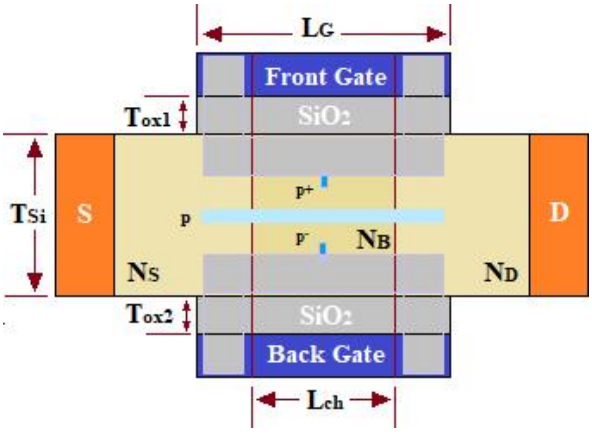

Figure 1. Illustration of proposed DG-MOSFET ρ-distinct slots structure

The Figure 2 illustrates that background doping of the silicon film for different ρ-based slot structure is regarded as intrinsic and includes 1 nm of top and bottom ρ slots of the gate stack with SiO2 p+ strained Si layer. The middle-ρ-slot gate stack, which has a thickness of 0.5 nm, is situated between the top and bottom gate stacks of uniform p insulating strained-Si. Additionally, a uniform p-strained Si layer with a high dielectric constant and a thickness of 1 nm is placed on top of the bottom SiO2 interfacial layer.

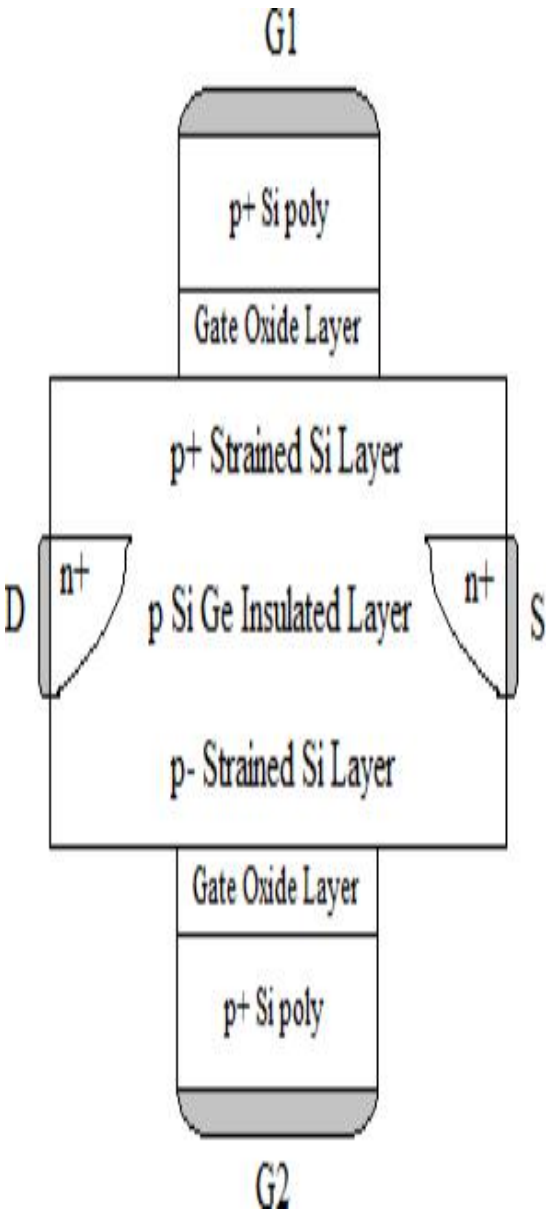

Figure 2. Illustration of proposed DG MOSFET ρ-strained Si structure

4.2. Model development

As seen in Figure 3, the DG MOSFET has a top p+ gate stack and a bottom p-gate stack with a high dielectric constant [26]. As the thickness of the bottom gate's high dielectric constant layer increases, the source-drain potential barrier decreases, raising the threshold level. The top and bottom gate stacks increase the drain current through the gate stack, which results in a high dielectric constant for the bottom gate and a threshold voltage and drain current that maintain the device dimensions at a steady pace. As a result, the dielectric constant potential barrier of the corresponding bottom gate stack decreases, which lowers the electron density and, for both gate stacks, lowers the threshold voltage. For DG MOSFETs with both p+ and p-gate stacks, the suggested model improves electron density and lowers the threshold voltage.

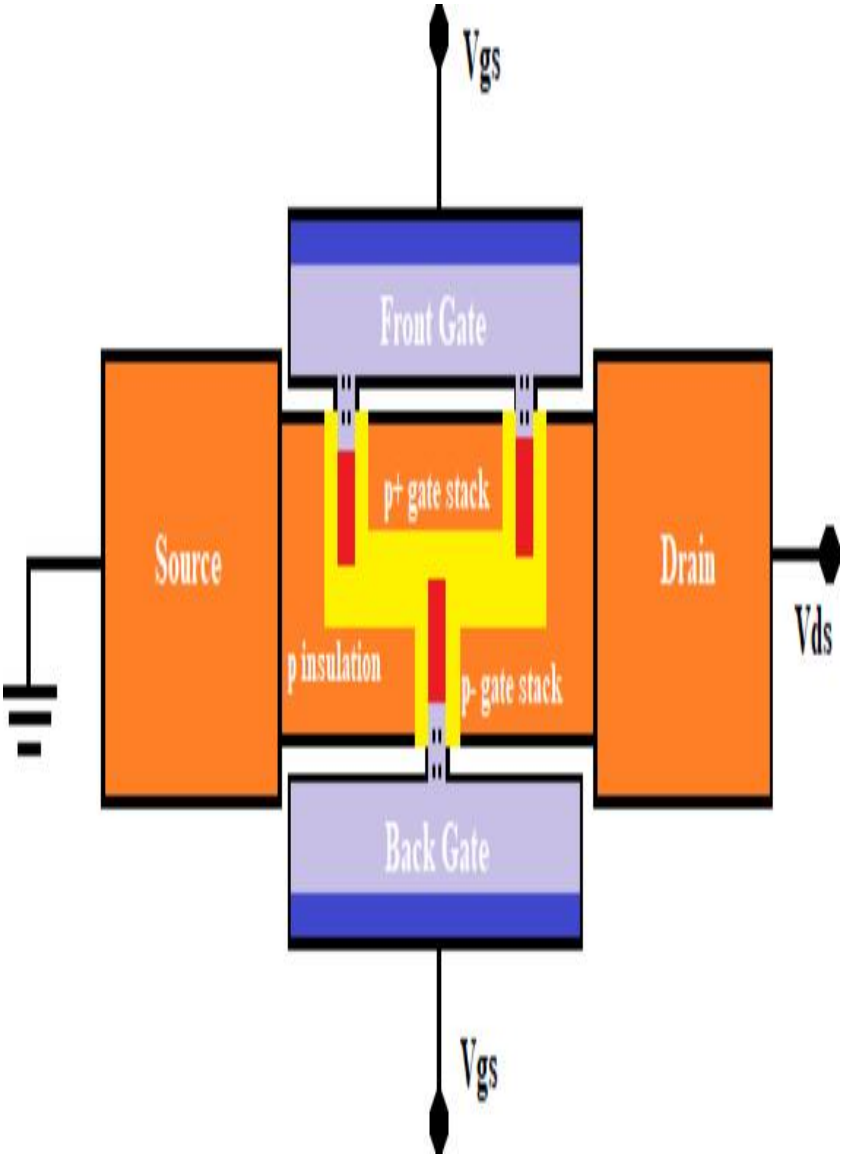

Figure 3. Illustration of proposed distinct ρ-based model of silicon N-channel double gate MOSFET

4.3. Model flowchart

Figure 4 shows the ballistic MOSFET flowchart when ballistic carrier transport is taken into account. The ultra-thin material sheet is used for the suggested DG MOSFET device design via one subband conduction. In Figure 5, the distinct ρ-based DG MOSFET design flow chart is shown, with crystalline grains made charged bodies through 1nm vertical cross-section area, having the charged density varying from 1 to 10 u, with u=1.28x10-12 C/cm. In the proposed DG MOSFET device design, subthreshold parameters and drain current characteristics were investigated in the presence of top and bottom charged distinct ρ-slots, which become asymmetric with the charge slots of dual-gate dielectric layers.

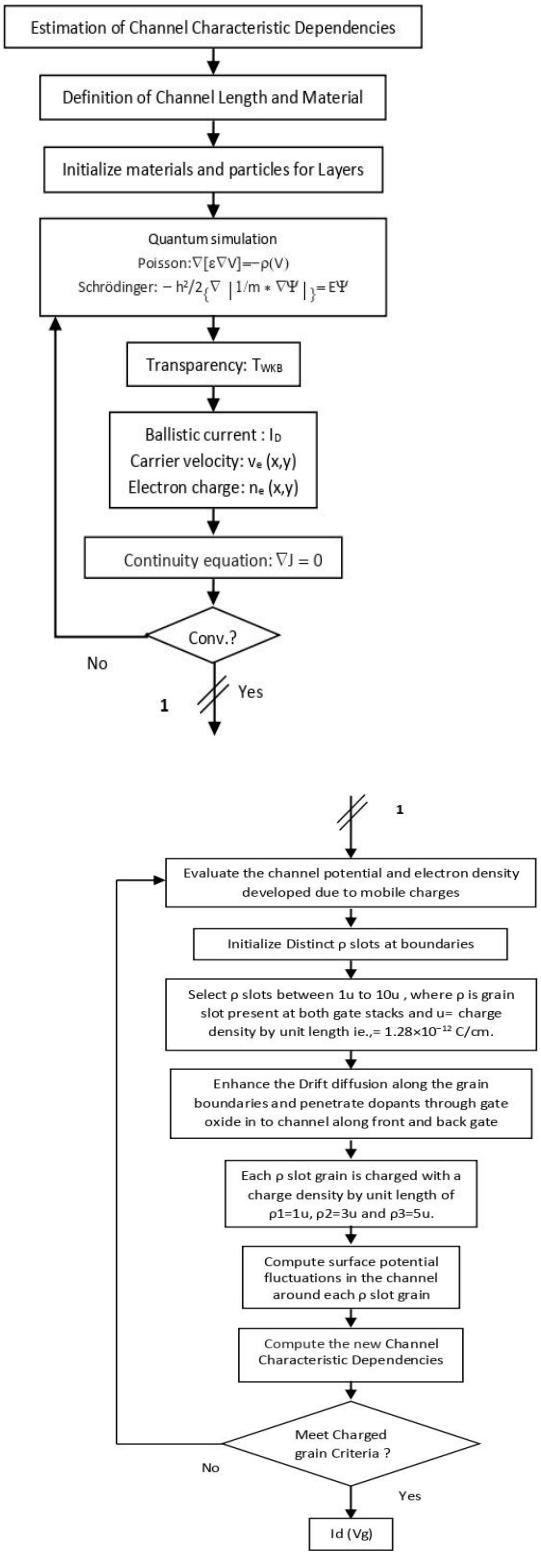

Figure 4. Flowchart of proposed DG MOSFET ballistic mechanism on Flow of ballistic DG MOSFET mechanism

Figure 5. Flowchart of proposed DG MOSFET carrier transport mechanism on Flow of distinct ρ-based DG MOSFET

4.4. Model mathematical representation

Here, the flowchart of the proposed DG MOSFET carrier transport mechanism is shown in Figure 5 as the flow of a unique ρ-based DG MOSFET mechanism is presented mathematically, and the flowchart of the ballistic MOSFET, which is shown in Figure 4 through ballistic carrier transport. Using carriers across the surface to scatter in to the gate doping regions with a layer capacitance as a dependent parameter near the field regions across distinct ρ-based front gate and back gate with proposed distinct ρ-based positions having the three grain sizes for ρ=1 u, ρ=3 u, and ρ=5 u, the proposed model is demonstrated in a two gate approach as front and back gate. This is a modified form of the ballistic complete model with a realistic DG MOSFET model. The drain to source current and the total gate current over the three grains are represented by (1) using the flux density concept.where is the front to back gate scattering coefficients, ^{5} is the front gate scatter carrier concentration

^{1}

from $_{=1}$ to $_{=3}$ and $_{=5}$ to $_{=3}$ and $_{3}$ is back gate scatter carrier concentration from $_{=3}$ to $_{=1}$ and $_{=3}$ to $_{=5}$. The parameters for ^{5} $_{1}$ $_{3}$ are given by (3).SIMULATION RESULTS AND DISCUSSION OF PROPOSED MODEL

During the simulation of proposed device, the analysis on effect of positions on the gate boundary is made. Since drift diffusion is constant at the boundary of device gate layers, only grains with a size of 1 nm are used. The ballistic approach is used to determine the characteristics of the number of three grains connected boundary surfaces, which depends on the predicted ρ value [27]. Table 1 displays the comparative device parameters taken into consideration in this investigation.

Table 1. Comparative device parameters considered for proposed distinct ρ-based DGMOSFET

Device parameters	Silicon MOSFET (CMOS)	GaAs MESFET	AlGaAs/GaAs MODFET	Distinct ρ-based DGMOSFET
Minimum channel length (μm)	0.1	0.2	0.18	0.2
Gate width (μm)	0.125	0.375	0.375	0.345
Doping (x 10^{18} / cm^3)	2.0	5.0	5.0	2.0
Threshold voltage (V)	0.4	0.2	0.25	0.2

Following proposed work achieved simulation results show three grain sizes for ρ=1 u, ρ=3 u, and ρ=5 u, representing two front gate grains and one back gate grain in the location of positions ρ=1 u, ρ=5 u, and position ρ=3 u respectively.

In Figures 6, 7, and 8 illustrate the total internal device capacitance variation in the 6 ρ=1 u, 7 ρ=3 u, and 8 ρ=5 u. Compare to traditional DG MOSFET designs for the comparison between performance of proposed approach and literature survey approaches, results achieved in the proposed DG MOSFET design are illustrated:

Because the positions in a traditional DG MOSFET are static and do not provide a desirable threshold voltage, the proposed design achieves a new result: the positions are moved through the device threshold voltage by varying the device capacitance with zero variations of the device gate grain polysilicon boundary in their displacement. b) Because the three gate drain voltages in traditional DG MOSFETs vary in either positive or negative gate values and do not provide desirable drain voltage and the intrusion detection systems (IDS) usages, the device's three gate drain voltage is chosen to be maximum at ρ=3 u location and increases its surface potential across ρ=1u and ρ=5u, causing the drain voltage to increase further. This is a new result achieved in the proposed design. c) The proposed design achieves a new result: the channel provides a uniform current flow in the crystalline structure of the DG MOSFET by reducing the channel gate device potential across the grain boundary. This is because in traditional DG MOSFET, the grain boundary is not taken into consideration for varying channel gate voltage variations, which do not provide desirable current flow and channel length variations. d) The front and back grain boundary charges in a traditional DG MOSFET are not equalized to provide uniform doping levels, nor do they provide desirable position estimations for gate to channel length distance and distinct slots to allocate with VG and VD variations. This new design achieves this goal by equalizing the boundary positions of these three grain charges with the underlying SiO2.

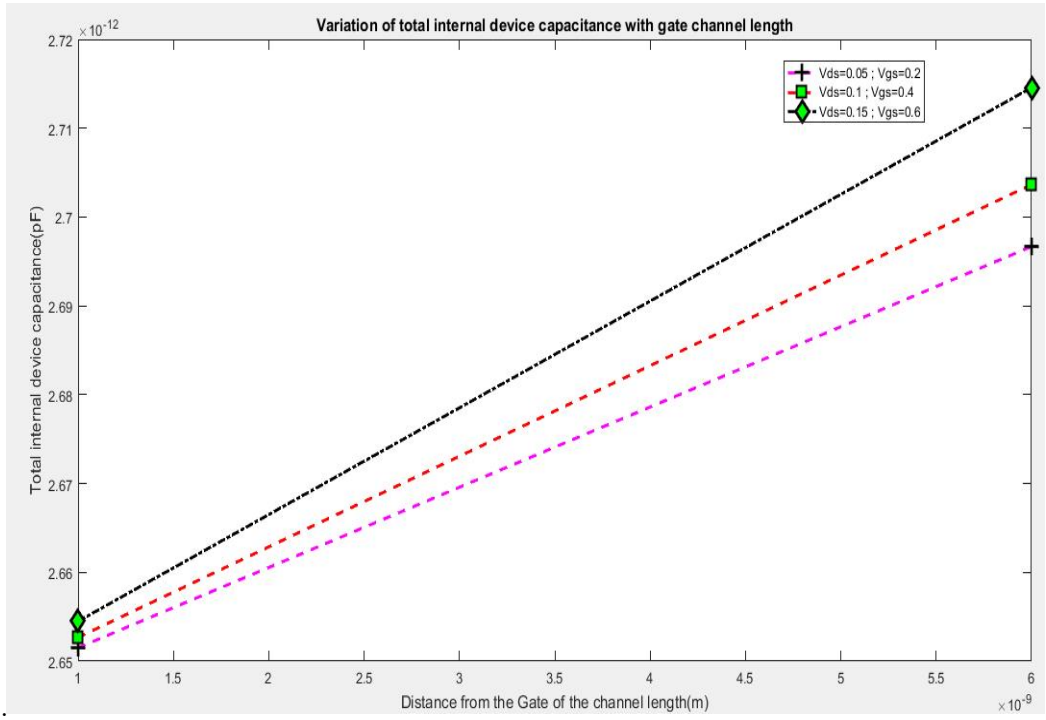

Figure 6. Channel characteristics for distinct ρ=1 u

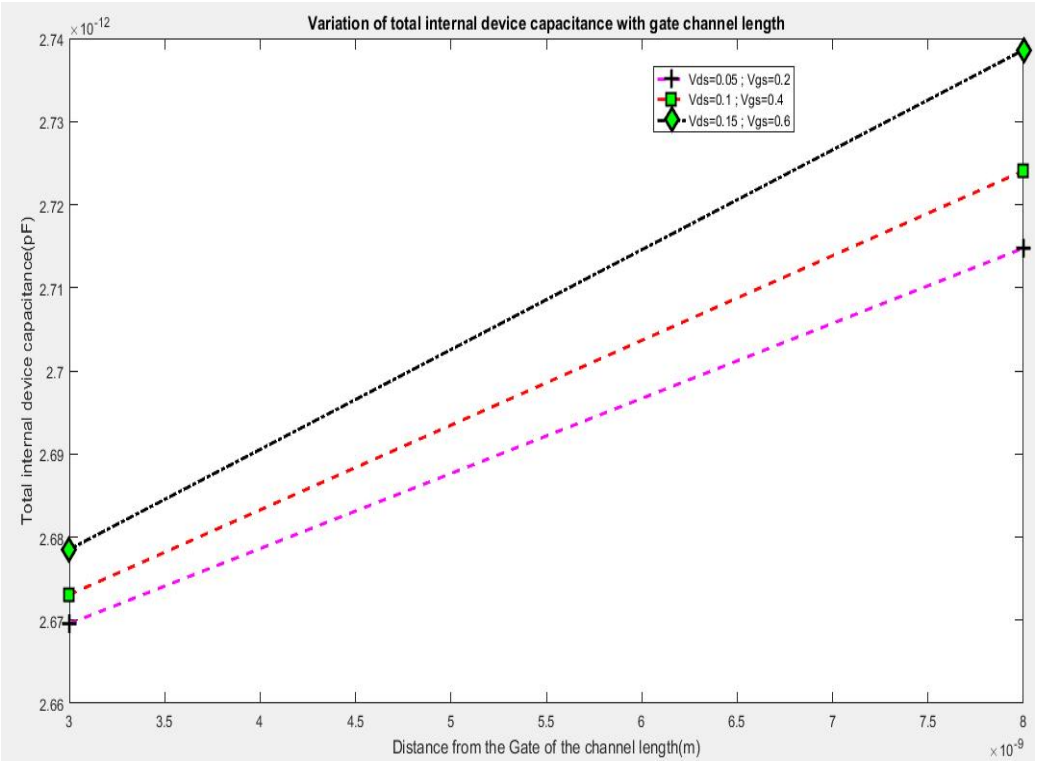

Figure 7. Channel characteristics for distinct ρ=3 u

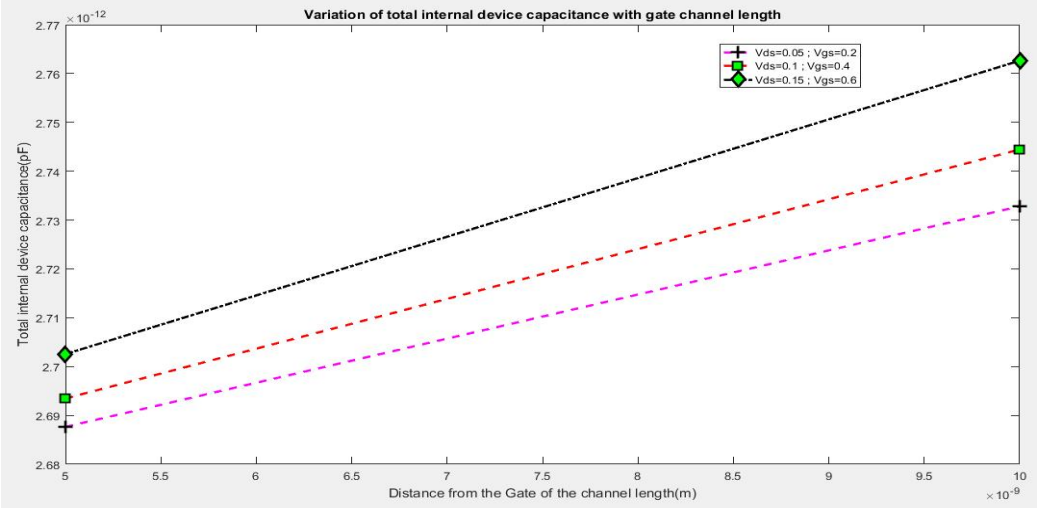

Figure 8. Channel characteristics for distinct ρ=5u

Figures 9 and 10 show the electrostatic charge distribution in the proposed distinct ρ-based MOSFET considering x=2 nm plane grain boundary, right below the semiconductor-insulator interface at VD=1 V and VG=1.5 V. The DG MOSFET crystalline structure is considered with dielectric constant values of 1, 3 and 5, as shown in Figure 6, through considering both ρ- front gate grains stacks and ρ- back gate grain stack. In Figure 11, the variations of threshold voltage with the device channel distance is made minimum potential across boundary of gate grains, and there is maximum potential changes across gate grains surfaces, with the varied distances of gate grains from 1-5 nm. Figure 12 also shows for gate level high grain bias potential variations of gates voltage with subthreshold drain current; ΔVg for different front and back gate voltages.

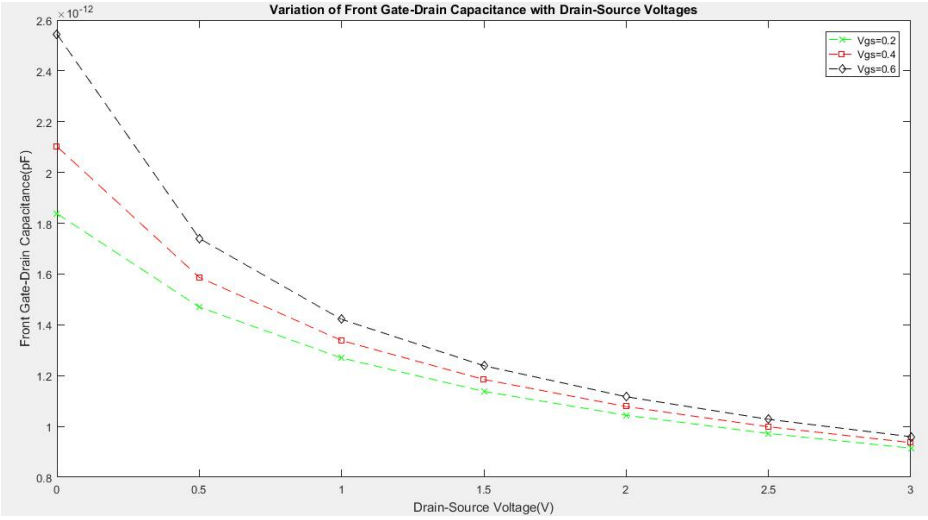

Figure 9. Voltage characteristics for distinct ρ-front stack

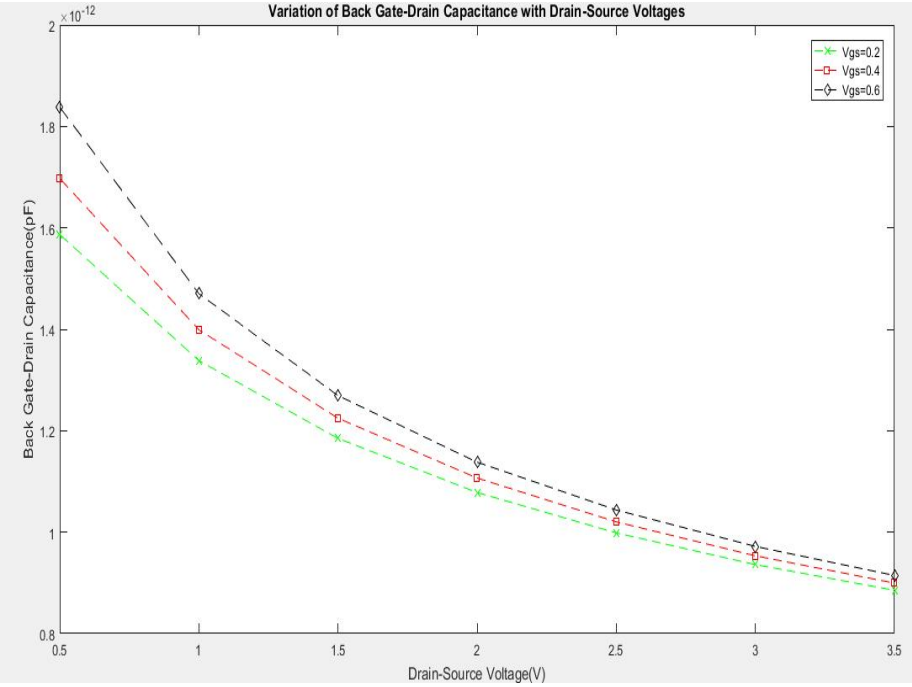

Figure 10. Voltage characteristics for distinct ρ-back stack

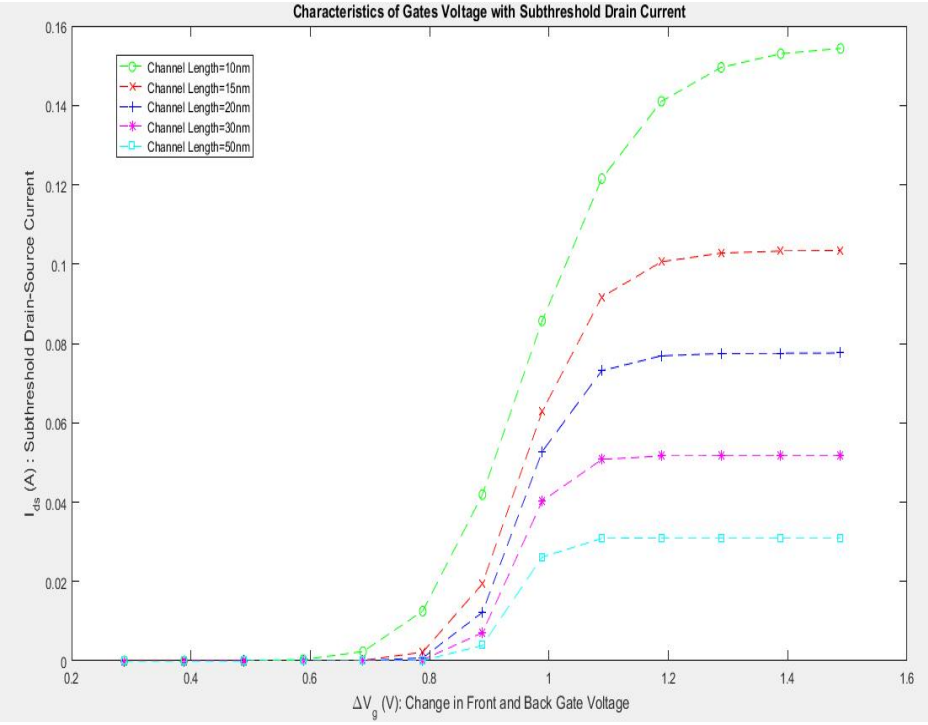

Figure 11. Variation of gates voltage with subthreshold drain current; δVg for different front and back gate voltages

Figures 12, 13, and 14 illustrate the 2-D potential distribution (VD=1 V and VG=1.5 V); Figure 12 for distinct ρ-front gate 2 stack slots; Figure 13 for distinct ρ-back gate 1 stack slots; Figure 14 for distinct ρ- front gate 2 and back gate 1 stack slots. In Figure 14, three grain charges with 1 u, 3 u and 5 u are positioned at a distance among the front gates and back gate device locations at the surface to penetrate the field under high dielectric layer positions.

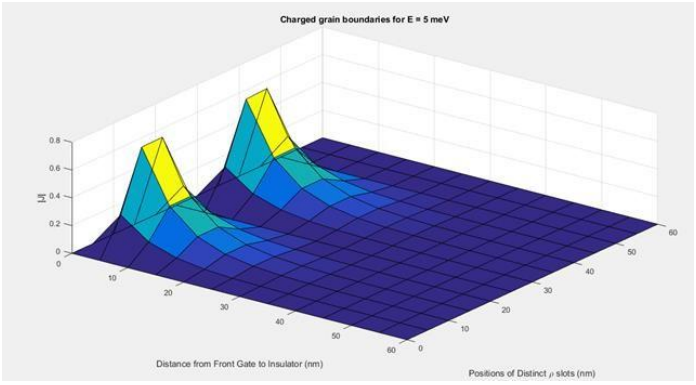

Figure 12. 2-D potential distribution (VD=1 V and VG=1.5 V) for distinct ρ-front gate 2 stack slots

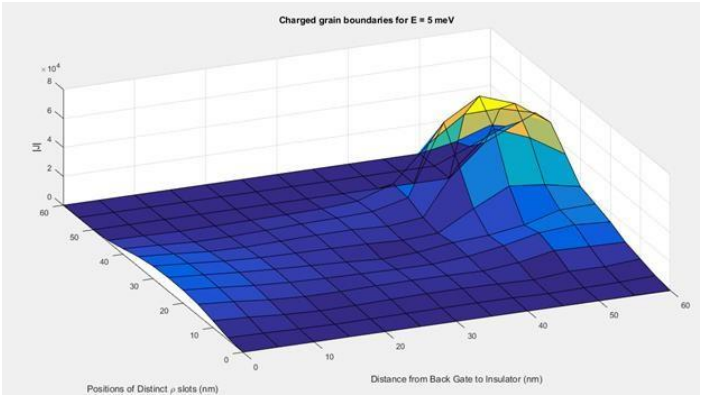

Figure 13. 2-D potential distribution (VG=VD=1.5 V) for distinct ρ-back gate 1 stack slots

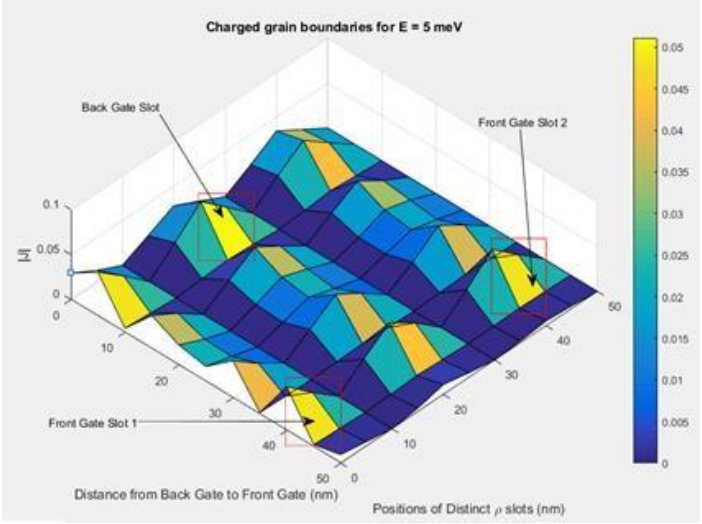

Figure 14. 2-D potential distribution (VG=VD=1.5 V) for distinct ρ-front gate 2 and back gate 1 stack slots

Figure 15 illustrates where the gate stacks-voltage variations are visualized for front gate and back gate on the surface gate stacks. Comparative analysis with TCAD as subthreshold slope modeling and proposed work simulation environment is illustrated in Table 2.

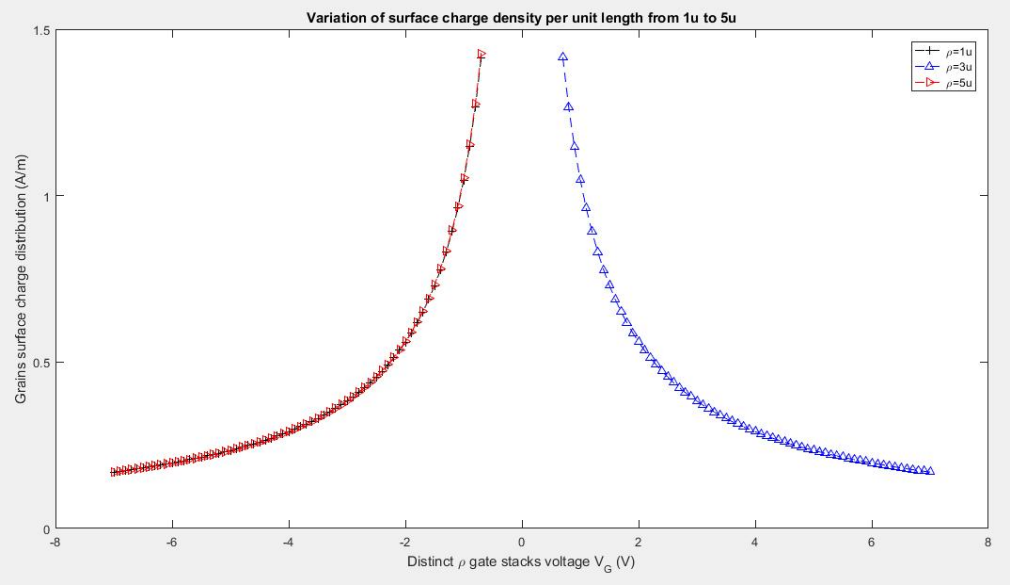

Figure 15. Variation of surface charge distribution for distinct ρ-front gate 2 (ρ=1 u and ρ=5 u) and back gate 1 (ρ=3 u) stack slots

Table 2. Comparative proposed distinct ρ-based model and TCAD as subthreshold slope modeling DG MOSFET

Variable	Front gate distance (nm)	Back gate distance (nm)	Gate length (nm) for Front gate distance	Gate length (nm) for back gate distance	V_{DS} (V)	Subthreshold slope (mV/dec)	DIBL (dec/V)
Subthreshold slope model	50	-	0.1	-	0.2	60	0.02
Proposed model	50	-	0.65	-	0.2	59.75	0.08
Subthreshold slope model	-	30	-	0.1	0.2	60	0.02
Proposed model	-	30	-	0.63	0.2	59.95	0.08

The effect of boundary potential made the subthreshold slope to reduce, even considering zero charge across device stack locations, in turn reducing the drain current to reduce, these limitations are made positive by shifting the current curve towards negative by adding a layer of high threshold voltage. From the above simulation results in 2D and 3D, it is proved that proposed work is having significant value in the implementation of planar DG MOSFET compared to available GAA, FinFETS, and tri-gate MOSFETs.

5. CONCLUSION

In a polycrystalline gate dielectric, the effects of the position-orientation of the border between three grains and the surface potential polysilicon doping close to the boundary in the channel area are examined. Understanding the electrical characteristics of silicon DG MOSFETs, including doping concentration, dimensions, total internal device capacitance, threshold voltage, and drain-source current, is made much easier by the proposed research project. Through the use of the

proposed theoretical simulation parameters by Possions equation, which has the advantage of using consistent and self-varying distinct ρ-front and back gate coupling in the estimated DG MOSFET gate regions by resolving the current drift and parasitic diffusion parameters through moderate gate doping, the presence of distinct ρ-front and back gate stack parasitic charge reduces the effect on I-V characteristics of the proposed DG MOSFET. By restricting the high dielectric typical DG MOSFET gate material in the proposed study, simulation results show that gate level potential changes are reduced by charges drifting along surfaces and boundaries. suggested task. By decreasing dielectric layer potential fluctuations, the suggested DG MOSFET's construction lowers its subthreshold value in drain current changes when compared to the conventional DG MOSFET subthreshold value. Thus, the contribution of a unique ρ-model to scaling DG MOSFET for thermal, static, and dynamic properties is the relevance of our suggested study effort.

6. FUTURE SCOPE

In this paper, distinct ρ-based DG MOSFET architecture model is proposed through ballistic DG MOSFET device for a compact DG MOSFET model by considering the SCEs parameters scaling and total internal device capacitance, which makes the device to degrades the off-state current and is particularly can be implemented in future DG MOSFET's using ballistic transport equation for further SCEs parameters analysis.

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