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Heart-rate Monitoring System Design and Analysis Using a Nios II Soft-core Processor

Wesam Ali[1], H. Ashour[2], Nimer Murshid[3]
[1,2,3]Department of Electrical and Electronic Engineering, International Islamic University Chittagong, Chittagong 4318, Bangladesh

Research Article

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***Abstract*—**A person's heart rate can reveal their level of health. A heart-rate monitoring device, such as an electrocardiogram (ECG) or a photoplethysmogram (PPG), can measure or record a person's heart rate in real time. This study implements a microprocessor system that is loaded with a heart-rate monitoring algorithm. The Nios II microprocessor system communicates with a pulse sensor and an analog-to-digital converter (ADC). The microprocessor system measures heart rate using a beat-finding algorithm. The functionality of the microprocessor system loaded with the algorithm is examined through an experiment. The findings indicate that the observed heart rate falls within the range of the typical human heart rate. SignalTap II from Quartus' software is used to view and study the signal flow within the microprocessor system. The suggested microprocessor system has a total power dissipation of about 218.26 mW, according to a power analysis report.

***Keywords*—PPG, Nios II, FPGA, heart rate, and pulse sensor**

I. INTRODUCTION

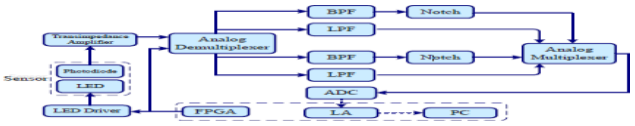
An apparatus that measures or records a person's heart rate in real time is called a heart-rate monitor. An individual's heart rate provides information about their health. This gadget uses either an electrocardiogram (ECG) or a photoplethysmogram (PPG) to measure physiological signals in order to do non-invasive heart-rate monitoring. Electrodes are applied to the patient's body for a certain amount of time in order to measure the electrical activity of the heart. Photoplethysmography uses an optical method to quantify the change in volume within an organ or tissue, such as the skin. Nowadays, a lot of heart-rate monitoring gadgets, particularly portable ones, use photoplethysmography. The heart rate and interbeat interval are computed using the PPG. The blood oxygen level (SpO2) can be detected by certain PPG-based methods. The majority of PPG-based systems employ a light-based sensor that measures light transmission and refraction. Particularly in pulse oximetry, several PPG-based devices employ multiple light wavelengths to increase PPG accuracy.

This work describes the implementation of a heart-rate measurement method in a microprocessor system that communicates with a pulse sensor and an ADC. A number of current pulse-based acquisition systems are covered in Section II, and the procedure for putting a microprocessor system equipped with a heart-rate measurement algorithm in a

The experimental configuration of a Field Programmable Gate Array (FPGA) that interfaces with an ADC and a pulse sensor. The system's experimental results are examined in Section IV. This paper is finally concluded in Section V.

II. LITERATURE REVIEW

In paper [1], a pulse oximetry system with motion artefact reduction based on Fourier analysis is introduced. Fig. 1 shows the block diagram of the proposed system, where the dotted boxes contain the sensor, the FPGA, the logic analyser (LA) and the personal computer (PC). In this system, a control signal is generated by the FPGA and sent to the PCB where analogue filtering is performed. In analogue filtering, the PCB receives the control signal from the FPGA and a signal from the photodiode that is converted from the light received from an LED. The signal is filtered and sent to the ADC where the signal will undergo digitalization. The digitalized signal is captured by a logic analyser and sent to the PC. Motion artefact reduction and SpO_2 calculation will take place in the PC. The purpose of motion artefact reduction is to reduce the effect of noise caused by the motion



artefact. The proposed system is used to calculate SpO_2 or blood-oxygen levels, as well as to perform PPG- signal acquisition.

Fig. 1. Block diagram of the proposed pulse oximetry system [1].

The authors in paper [2] present a high-speed pulse data acquisition system based on an FPGA and a USB interface. The acquisition system consists of an HK-2000G pulse transducer, a Cyclone II series FPGA chip, an FTDI USB communication interface chip, a memory chip, an amplifier and filter circuits, a 16-bit A/D converter and a PC. Fig. 2 illustrates the block diagram of the pulse data acquisition system. The pulse signal is captured in real time from the sensor through the ADC. The signal is sampled by the ADC and stored in the PC's memory by the FPGA. The FPGA allows the data to be transferred to the PC through the USB interface, where the data is presented on the screen by using the PC's software. The system is developed to help doctors to analyse the pulse condition's information in real time.

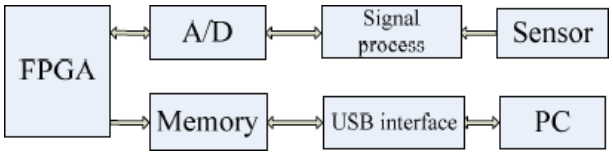


Fig. 2. Block diagram of the proposed pulse data acquisition system [2].

An FPGA-based Remote Pulse Rate Detection system is introduced by the authors in paper [3]. The proposed system uses the photoplethysmographic imaging method for pulse detection, where a low-cost digital camera is used as an image sensor for the system. A block diagram of the proposed system is illustrated in Fig. 3, showing the FPGA, the camera, an LCD and an SD card. The FPGA consists of a video pipeline and the proposed algorithm. The video pipeline carries out image processing from the camera. The proposed algorithm is a novel algorithm which is used for pulse rate measurement. In this proposed system, the pulse rate can be measured by placing a palm 20 cm away from the camera.

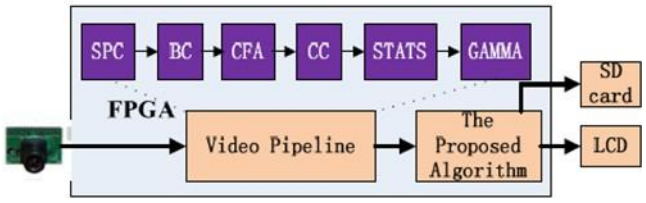


Fig. 3. Block diagram of proposed system [3].

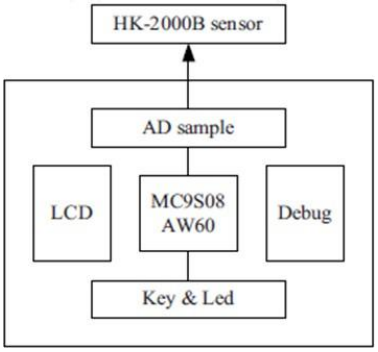


Fig. 4. Block diagram of the proposed pulse monitoring system [4].

In paper [4], a pulse monitoring system based on a feedback algorithm is introduced. In this system, a low power, 8-bit microcontroller with a built-in ADC is used. Besides the microcontroller, the system consists of an HK-2000B-type pulse sensor, an LCD display, LEDs, a Debug interface and buttons. The pulse monitoring system is illustrated in Fig. 4. A feedback algorithm is used in the microcontroller system to improve the detection accuracy of the pulse signal. The results show that the feedback algorithm does not reduce the accuracy of the system.

The authors in paper [5] implemented a pulse signal detection system with Bluetooth transmission. The structure of the system is illustrated in Fig. 5 and it consists of a pulse sensor, an Arduino microcontroller board, Bluetooth modules and a PC management platform. In the proposed system, the pulse signal is sampled by a built-in ADC of the Arduino microcontroller after the signal has been filtered and amplified. After the pulse signal is digitalized, data processing will be

carried out on the pulse signal in the Arduino microcontroller board to calculate the pulse rate and time between heartbeats. The calculated results will be transmitted to the PC management platform though the Bluetooth modules. The PC management platform displays the calculated result and the pulse signal on the screen using processing software. Some of the related data are stored in the form of text file on the PC for further research.

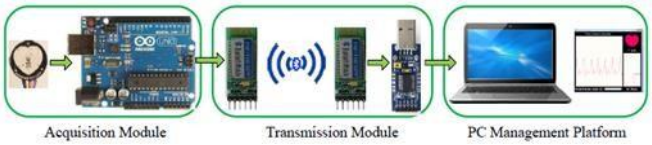


Fig. 5. Structure of the pulse signal detection system [5].

TABLE I
COMPARISON OF EXISTING MICROPROCESSOR SYSTEMS WITH AN ADC FOR BIOMEDICAL APPLICATION

Reference	[1]	[2]	[3]	[4]	[5]
System	PC	PC	Dedicated control block	8-bit µc	Arduino µc and PC
ADC	Yes	16-bit ADC	No	µc Built-in	µc Built-in
Application	Pulse oximetry	Pulse analysis	Remote pulse rate measurement	Pulse monitoring	PPG signal analysis
Algorithm	SpO_2 calculation and motion artifact reduction	Hilbert-Huang transform	Image processing and novel pulse rate measurement algorithm	Feedback algorithm	Heart rate and time between heartbeats calculation
Hardware	FPGA, ASIC, PC	FPGA, ASIC, PC	FPGA	ASIC	ASIC, PC

Several existing pulse-based acquisition systems are reviewed in this paper. The features of the existing systems are tabulated in Table I. Based on Table I, some of the systems used the PC as a main control or platform to execute the algorithm and display the results on the screen of the PC, while some of the acquisition systems are microcontroller-based systems. However, a custom design controller module is used in the acquisition system. Among the existing systems, most systems contain an ADC, such as a built-in ADC and an ADC chip. Pulse-based acquisition systems are normally able to detect pulse rates. However, some of the pulse-based acquisition systems are also able to detect blood oxygen levels. The algorithms of the systems are various, and the choice of algorithm depends on the designer of the system. The algorithm may include results' calculation, filtering and noise reduction. The choice of the system's hardware depends on the designer, and may integrate an FPGA or application-specific integrated circuit (ASIC), interface with a PC or have a combination of the two.

III. METHODOLOGY

In the previous section, the existing heart-rate monitoring systems are discussed; this section explains the algorithm for heart-rate monitoring and the proposed microprocessor system that interfaces with an ADC and a pulse sensor. The proposed system is a Nios II microprocessor system that is implemented on an FPGA to interface with the ADC and the pulse sensor. The system architecture consists of a Nios II economy version

soft-core processor, two 32 Mb SDRAMs with an SDRAM controller, a 32 Kb on-chip memory, a timer module, an Avalon bus, a Joint Test Action Group (JTAG), a universal asynchronous receiver transmitter (UART) and the general input and output (GPIO). Fig. 6 shows the block diagram of the proposed microprocessor system with an ADC and a pulse sensor. In this system, the interval period of the timer module is 500µs. The ADC used for signal conversion between the pulse sensor and microprocessor system is an 8-bit microprocessor-compatible ADC integrated circuit (IC) from National Semiconductor, ADC0804. The ADC0804 is an 8-bit successive approximation ADC and has one differential analogue voltage input [6]. In the proposed system, ADC0804 receives an analogue input from the pulse sensor and provides an 8-bit digital output to the microprocessor system through the GPIO. 150pF capacitor and a 10K ohm resistor is used as a clocking circuit for the ADC0804, which allows the ADC to use self-clocking instead of an external clock. With this configuration, the analogue input is converted into a digital output automatically by the internal clock. A conversion time of approximate 100µs is required for the analogue input to be converted into 8-bit digital data successfully [6].

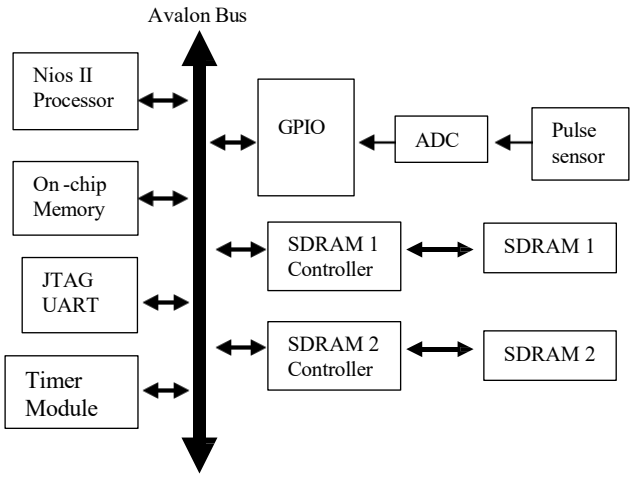


Fig. 6. Block diagram of a microprocessor system with an ADC and a pulse sensor.

In this work, a non-invasive heart-rate monitoring sensor is used, which is a PPG-based pulse sensor. The pulse sensor is an optical-based heart-rate sensor with the model name SN-PULSE from Cytron Technologies. This pulse sensor operates by emitting light from the green LED to human skin and tissue, and receives the reflected light from the skin and tissue with a photodiode. The pulse sensor interfaces easily with the microprocessor system or microcontroller, which operates with a 5V supply and does not require an external circuit in order for the sensor to operate. The pulse sensor has built-in amplification and a noise-cancellation circuit that improves the output signal. The sensor has a single analogue output and the output voltage range is between 0V to 5V, where the output signal amplitude is dependent on the light reflected or absorbed by the skin and tissue, while the sensor is attached to a human finger.

The analogue output from the pulse sensor is converted into 8-bit digital output data, and sent to the microprocessor system by the ADC0804 IC. It interfaces with a microprocessor using an 8-bit parallel data port. The ADC0804 is selected due to the fact that it is 8-bit microprocessor-compatible and it is able to receive an analogue-input voltage range that is the same as the analogue output of the pulse sensor. The circuit configuration of the ADC0804 is set in a free running configuration. Fig. 7 shows the free running configuration of the ADC0804 for this work. In this configuration, an RC circuit that consists of a

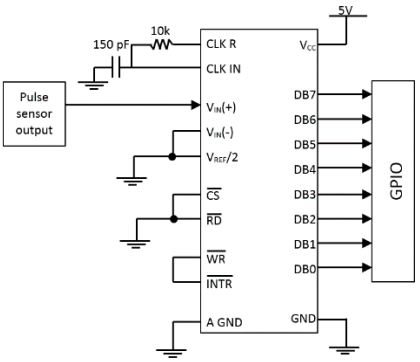


Fig. 7. The free running configuration of the ADC0804.

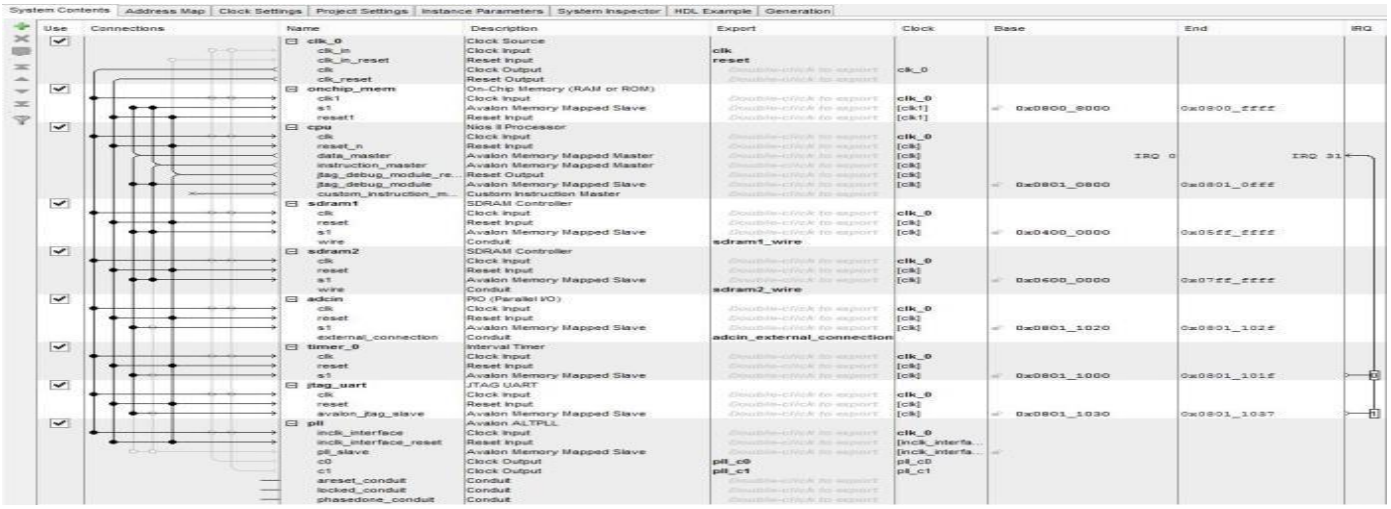


Fig. 8. System interconnection of the proposed microprocessor system in Qsys

The microprocessor system's design is developed by integrating the modules or components together, using the Qsys tool from the Quartus II software. The system's design is compiled and synthesized by using Quartus II software. Its I/O contact is assigned to the system design by Quartus II based on the Cyclone II EP2C70F896C7 FGPA chip. The synthesized system design is downloaded to a Cyclone II EP2C70F896C7 FGPA chip in the Altera DE2-70 Board by using the Quartus II programmer. Fig. 8 shows the system interconnection of the proposed microprocessor system in the Qsys tool. The system interconnection is based on the block diagram of the microprocessor system illustrated in Fig. 6. In this system, a phase-locked loop (PLL) module is used to provide two 50 MHz -0.3 ns shifted clocked pulses to two 32Mb SDRAMs.

The Nios II Software Build Tool is a tool chain for Nios II processor where it is used to compile an application program for the processor, provide a driver and hardware abstraction layer (HAL) support to the processor and download the application's program-to-program memory of the microprocessor system. In this work, the application program is developed based on the heart-rate monitoring algorithm and data acquisition system. In the application program, a timer interrupt is activated to perform periodic sampling on the analogue input from the pulse sensor by receiving 8-bit digital output data from the ADC, and storing the data on the SDRAM 1. Since the timer interval period is 500µs, the sampling rate of the microprocessor system is 2kS/s. By setting the timer interrupt, the microprocessor system will sample the data consistently. Once a certain amount of data is stored (1000 data points), the heart-rate monitoring algorithm is carried out by the microprocessor system and the results, such as an inter-beat interval (IBI) and beats per minute (bpm), are stored in the SDRAM 2. At same time, the results are shown in the Nios II console through JTAGUART.

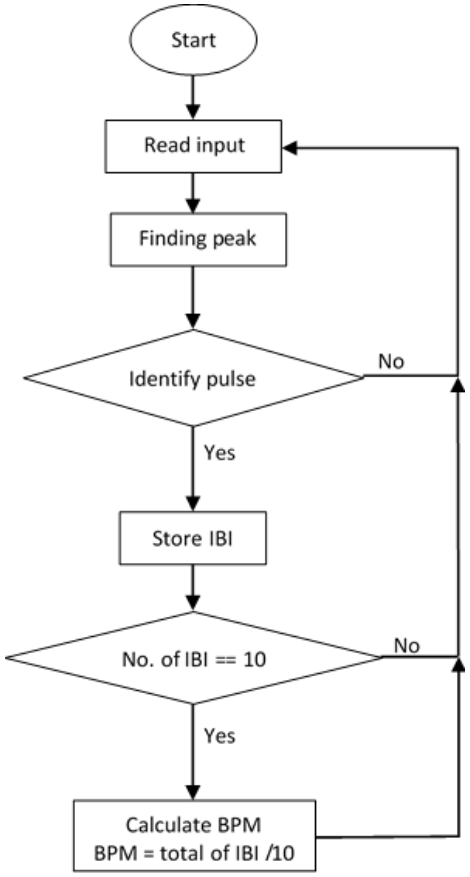


Fig. 9. Flow chart of the beat-finding algorithm for heart-rate monitoring.

The algorithm used for heart-rate monitoring is a beat-finding algorithm. The beat-finding algorithm is a peak detection-based algorithm and the algorithm is based on a "PULSE SENSOR AMPED" website [7]. Fig. 9 shows a simplified flow chart of the beat-finding algorithm for the microprocessor system. The algorithm starts by reading the input data from the SDRAM 1. A peak-finding process will be carried out on the data read from the SDRAM 1. By using the detected peaks, a pulse can be identified based on amplitude of the peaks and the duration between the peaks. The process is repeated until a correct pulse is determined. Once the correct pulse is identified, the IBI is calculated by measuring a period of the pulse between the two nearest peaks and the IBI value is stored in the SDRAM 2. When 10 IBI values are stored, the

BPM is calculated by dividing the total of the IBI value by 10 (Total IBI / 10) and the BPM is stored on the SDRAM 2. In the Nios II console, IBI and BPM values are presented. Fig. 10 shows the pseudocode for the beat-finding algorithm.



Fig. 10. Pseudocode.

An experiment is set-up to test the functionality of the microprocessor system and beat-finding algorithm. The microprocessor system's design is loaded onto the FPGA board. The FPGA board with an ADC and a pulse sensor is illustrated in Fig. 11. A 25-year-old male student is used as the test target for the heart-rate monitoring. In this experiment, the pulse sensor is attached to the finger for heart-rate measurement.

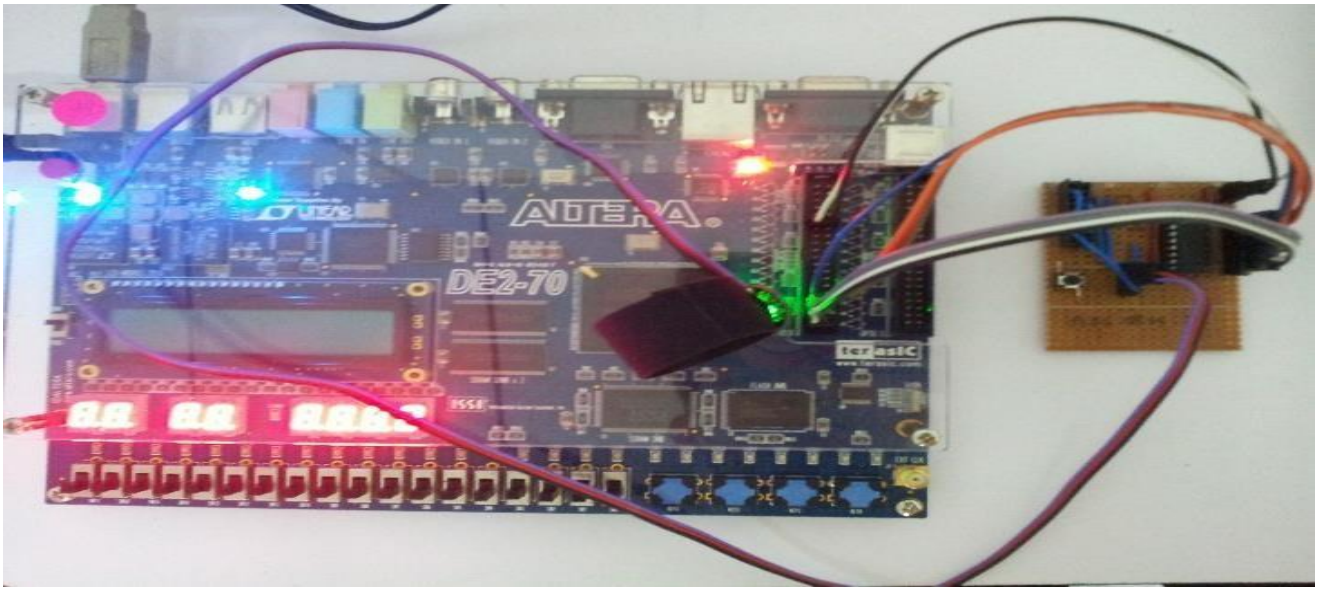


Fig. 11. Microprocessor system in the FPGA board with an ADC and a pulse sensor.

IV. Results And Discussion

In this section, the results of an experiment with the heart-rate monitoring system are observed and discussed. In addition, the signal flow within the microprocessor system is discussed in detail. An experiment is set-up to measure the heart rate of a 25-year-old male student, with the pulse sensor attached to a finger. The student is in a resting position (sitting on a chair). From the experiment, the results show that the bpm range is between 68 bpm and 82 bpm. This is within the range of the average resting heart rate, which is between 60 bpm to 100 bpm. This proved that the heart-rate monitoring system is working as intended. In Fig. 12, the IBI and the bpm values are presented in the Nios II console.

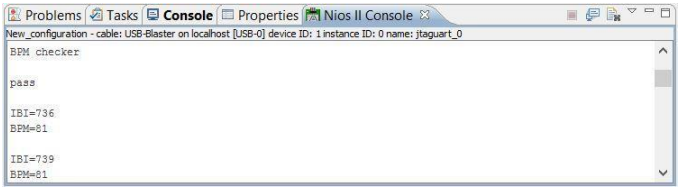


Fig. 12. Nios II console presenting the IBI and bpm values of the target male student.

In order to observe the signal flow in the microprocessor system, SignalTap II from the Quartus II software is used to capture the data transfer within the microprocessor system. SignalTap II is an embedded logic analyser that captures and displays signals in the circuit design. In SignalTap II, all the inputs and outputs are probed to capture the signal flow. The inputs and outputs are the interfaces between the microprocessor and the SDRAMs, and the interfaces between the microprocessor and the ADC, repectively. The clock source for the signal tap is set using the 50MHz clock source from the DE2-70 board. The data-sample depth is 8k, and the storage qualifier is set as a transitional type. In this embedded logic analyser, three situations are selected to observe the signal flows that are storing data from the ADC to the SDRAM 1 (`DRAM0`), reading data from the SDRAM 1 and storing the resulting data to the SDRAM 2 (`DRAM1`). The waveform in Fig. 13, Fig. 14 and Fig. 15 are the captured data obtained by using the SignalTap II embedded analyser in real time. Fig. 13 shows the write operation on the SDRAM 1 by storing the data obtained from the ADC. The green box in Fig. 13 shows the write operation on the SDRAM 1 with data from the ADC output. In Fig. 13, the ADC output (`ADCIN`) value is 7DH. When the write operation on the SDRAM 1 is carried out, the write enable signal (`DRAM0_WE_N`), the column address strobe (`DRAM0_CAS_N`) and the chip select signal (`DRAM0_CS_N`) are set to low, while the row address strobe (`DRAM0_RAS_N`), clock enable (`DRAM0_CKE`) and system clock input (`DRAM0_CLK`) are set to high [8]. With the address bus (`DRAM0_A` and `DRAM0_BA`), Data I/O mask (`DRAM0_LDQM0` and `DRAM0_UDQM1`) and data bus (`DRAM_DQ`) being set, the data are written onto the SDRAM [8].

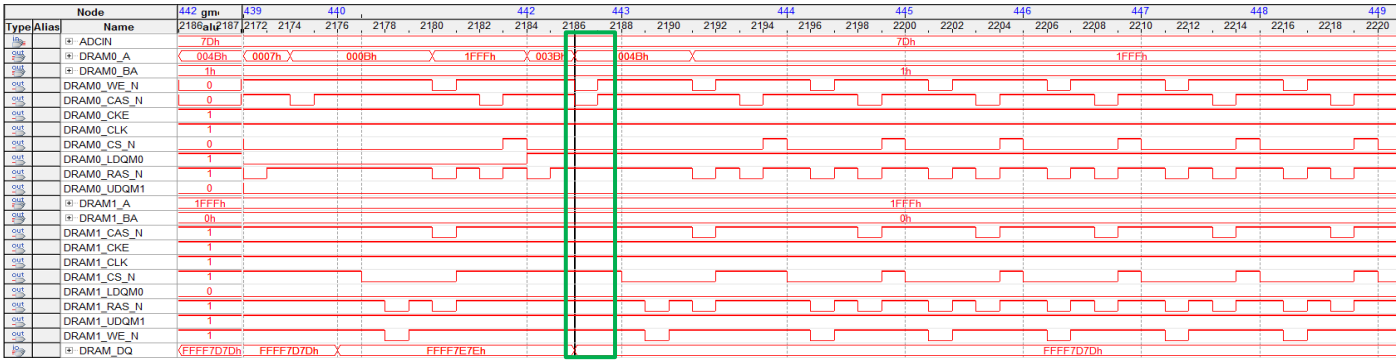


Fig. 13. Captured waveform of storing data from ADC output to SDRAM 1 using SignalTap II

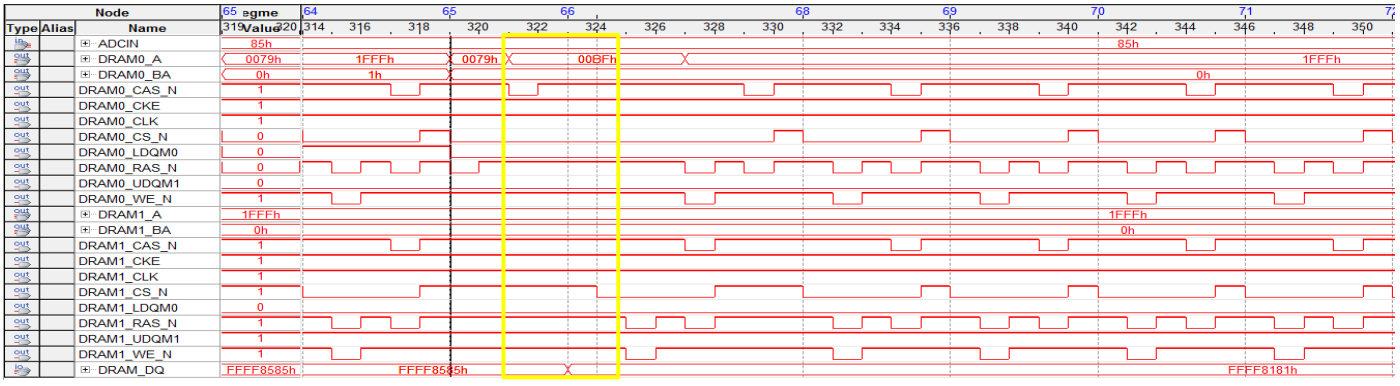


Fig. 14. Captured waveform of reading data from the SDRAM 1 by using SignalTap II

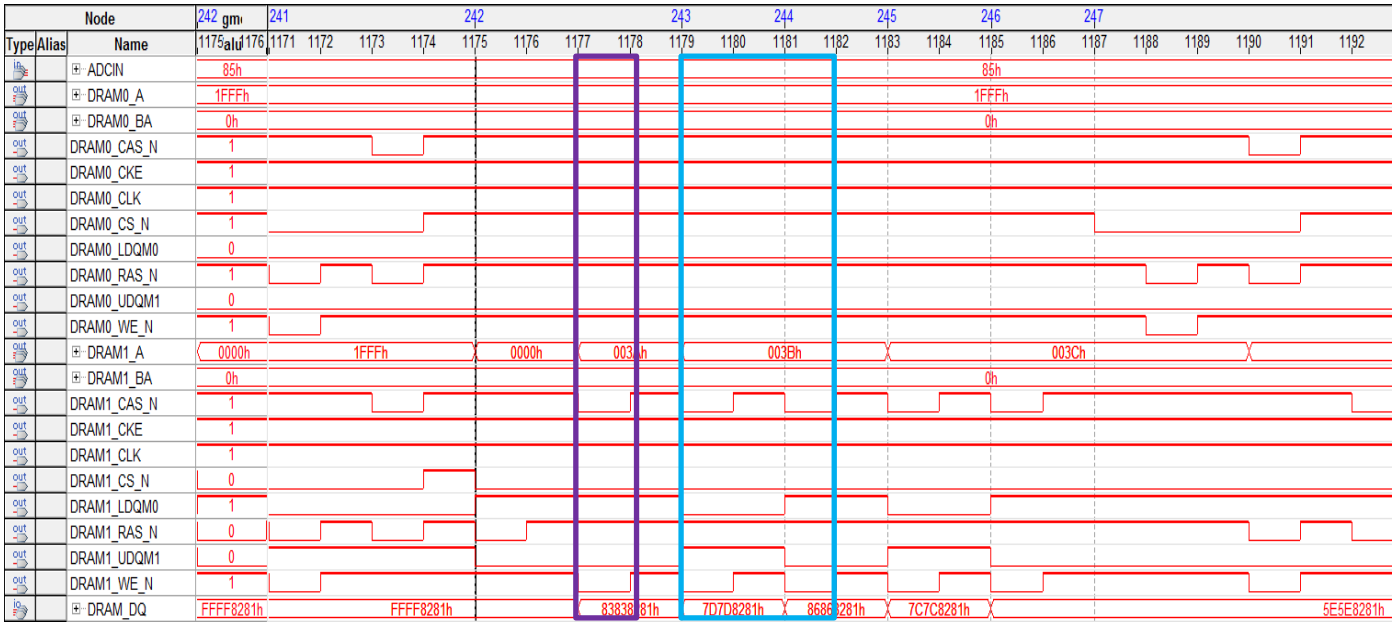


Fig. 15. Captured waveform of storing resulting data to the SDRAM 2 by using SignalTap II

In Fig. 14, the captured waveform of the read operation on the SDRAM 1 is presented. The yellow box in Fig. 14 shows the 8-bit read operation on the SDRAM 1 with the address of 00BFH to the obtained data value of 81H (since `DRAM_DQ` is a 32-bit bus, the two least significant bytes are the data value). The read operation is similar to the write operation explained previously, but with the difference that the write enable signal (`DRAM0_WE_N`) remains high [8]. In this read operation, there is a latency delay after the write operation has been carried out. The purpose of reading data from the SDRAM 1 is to allow the algorithm to run on the data. In Fig. 15, the captured waveform presents the write operation on data storing in the SDRAM 2 (`DRAM1`). The purple box shows the write operation of data 83H on the SDRAM 2 with the address of 003AH (since `DRAM_DQ` is a 32-bit bus, the fifth and sixth byte from the least significant byte are the data values for the SDRAM 2). The blue box shows the write operation of data value 7D86H on the SDRAM 2 with the address 003BH. From the purple box in Fig. 15, the write operation is carried out twice with the data I/O mask bus (`DRAM1_LDQM0` and `DRAM1_UDQM1`) being toggled. This is to allow the high byte value being stored in the SDRAM 2 before the lower byte value is stored. The writing operation in Fig. 15 shows that the resulting data are stored to the SDRAM 2.

TABLE II
TOTAL LOGIC ELEMENTS AND POWER DISSIPATION FOR THE PROPOSED MICROPROCESSOR SYSTEM

Total Logic Elements	**Total Thermal Power Dissipation**	**Core Static Thermal Power Dissipation**	**I/O Thermal Power Dissipation**
4,995	218.26 mW	155.03 mW	49.53 mW

Based on the compilation report, the total number of logic elements for the proposed microprocessor system is around 4,995. From the PowerPlay Power Analyzer report, the total thermal power dissipation for the proposed system is 218.26 mW, where the core static thermal power dissipation is around
155.03 mW and the I/O thermal power dissipation is 49.53 mW. Table II tabulates the total logic elements and the power dissipation for the proposed system with different timer

module periods. The PowerPlay Power Analysis is carried out using 12.5% of the default toggle rate for the input I/O signal, and the toggle rates of the remaining signals are vectorless estimated.

V. CONCLUSION

This paper describes the implementation of a microprocessor system loaded with a heart-rate measuring method. FPGA hardware is used to implement the microprocessor system, which communicates with a pulse sensor and an ADC. A literature review discusses a number of current microprocessor systems that use a pulse signal-based sensor. The functionality of the microprocessor system loaded with the algorithm is examined through an experiment. The findings demonstrate that the observed heart rate falls within the typical range of a human heart. The microprocessor system's signal flow is monitored and examined. The suggested microprocessor system has a total power dissipation of about 218.26 mW, according to the power analysis results. The heart-rate monitoring system will be developed into a portable gadget that enables real-time heart-rate monitoring in the future.

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